Numerical Integration Methods for Electric Circuit Simulation Packages

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Automatic generation and numerical integration of network equations are the core of industrial TCAD packages. These tools allow short design cycles of VLSI circuits, e. g. dynamic memories. But this modeling approach leads to systems of differential and algebraic equations (DAEs) with redundant variables. DAEs are characterized by the *index*. Roughly spoken, the index is a measure for the additional effort which will arise by solving a DAE. The analytical and numerical problems are getting worse with a larger index.

SPICE, one of the most popular electric circuit simulators, and its successors use BDFs as integration schemes. The stepsize control of BDF is successfully adapted to problems of index-0 and index-1. We discuss the *index* problem in chip simulation and show alternative integration methods.

In general not all parts of large integrated circuits are uniformly active during simulation: large parts of the circuit remain latent during a certain time interval. This latency is exploited by a multirate ROW approach, which uses different step sizes for the active and latent part of the circuit.

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