\$<, a so called macro, is short for the Fortran file. Sometimes we wish the recompile all files (we may have changed One can use variables in make, here OBJS and FFLAGS. \$(FFLAGS) for example). It is common to have the target clean. When having several targets we can specify the one that should OBJS = main.o sub.o be made: FFLAGS = -03run: \$(OBJS) OBJS = main.o sub.o g95 -o run \$(FFLAGS) \$(OBJS) FC = g95 FFLAGS = -03.SUFFIXES: .f90 run: \$(OBJS) .£90.o: g95 -c \$(FFLAGS) \$< \$(FC) -o run \$(FFLAGS) \$(OBJS) OBJS (for objects) is a variable and the first line is an assignment # Remove objects and executable to it. \$(OBJS) is the value (i.e. main.o sub.o) of the variable clean: OBJS. FFLAGS is a standard name for flags to the Fortran comrm -f \$(OBJS) run piler. I have switched on optimization in this case. Note that we have changed the suffix rule as well. .SUFFIXES: .f90 .f90.o: Make knows about certain variables, like FFLAGS. Suppose we \$(FC) -c \$(FFLAGS) \$< would like to use the ifort-compiler instead. When compiling the source files, make is using the compiler whose name is stored Without -f, rm will complain if some files are missing. in the variable FC (or possible F90 or F90C). We write: We type: OBJS = main.o sub.o FC = ifort % make clean FFLAGS = -03rm -f main.o sub.o run run: \$(OBJS) \$(FC) -o run \$(FFLAGS) \$(OBJS) .SUFFIXES: .f90 .f90.o: \$(FC) -c \$(FFLAGS) \$< It is usually important to use the same compiler for compiling and linking (or we may get the wrong libraries). It may also be important to use the same Fortran flags. 53 54Suppose we like to use a library containing compiled routines. For the assignments it is easiest to have one directory and one The new makefile may look like: makefile for each. It is also possible to have all files in one directory and make one big makefile. OBJS = main.o sub.o FC = g95 OBJS1 = main1.o sub1.o FFLAGS = -03OBJS2 = main2.o sub2.o LIBS = -lmy\_library CC = cc CFLAGS = -03LIBS1 = -lm run: \$(OBJS) \$(FC) -o run \$(FFLAGS) \$(OBJS) \$(LIBS) LIBS2 = -lmy\_library .SUFFIXES: .f90 all: prog1 prog2 .f90.o: \$(FC) -c \$(FFLAGS) \$< prog1: \$(OBJS1) \$(CC) -o \$@ \$(CFLAGS) \$(OBJS1) \$(LIBS1) If you are using standard functions in C sin, exp etc. you must prog2: \$(OBJS2) use the math-library: \$(CC) -o \$@ \$(CFLAGS) \$(OBJS2) \$(LIBS2) cc ... -lm clean: The equivalent makefile for C-programs looks like: rm -f \$(OBJS1) \$(OBJS2) prog1 prog2 OBJS = main.o sub.o When one is working with (and distributing) large projects it CC = CC is common to use make in a recursive fashion. The source code CFLAGS = -03is distributed in several directories. A makefile on the top-level LIBS = -lmy\_library -lm takes care of descending into each sub-directory and invoking make on a local makefile in each directory. run: \$(OBJS) \$(CC) -o run \$(CFLAGS) \$(OBJS) \$(LIBS) There is much more to say about make. See e.g. the O'Reillybook, Robert Mecklenburg, Managing Projects with GNU Make, clean: 3rd ed, 2004. rm -f \$(OBJS) run

# Computer Architecture

A very simple (and traditional) model of a computer:  $\sim$ 

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Why this lecture?		CPU	Memory bus	Memory	I/O bus	I/O devices	
Some knowledge about computer architecture is necessary:							
• to understand the behaviour of programs	The CDU contains the ALLI suithmetic and logic unit and the						
$\bullet$ in order to pick the most efficient algorithm	The CPU contains the ALU, arithmetic and logic unit and the control unit. The ALU performs operations such as $+, -, *, /$ of						
• to be able to write efficient programs	intege The c	ers and Boo	olean opera	tions.	ahing door	ding and	
• to know what computer to run on (what type of architecture is your code best suited for)	execu The n	ting instru	tions. res instruct	ions and da	ata. Instru	ctions are fe	etched
• to read (some) articles in numerical analysis	to the	CPU and	data is mo	ved betwee	n memory	and CPU ı	using
• when looking for the next computer to buy (and to understand those PC-ads., caches, GHz, RISC)	buses. I/O-d	evices are	disks, keyb	oards etc.			
The change of computer architecture has made it necessary to re-design software, e.g Linpack $\Rightarrow$ Lapack.	The C • PC	CPU contai C, program	ns several counter, c	registers, s contains the	uch as: e address o	f the next	
	ins	struction to	be execu	ted			
	• IR	, instructio	on register	the execu	ting instru	ction	
	• ad	dress regis	ters				
	• da	ta register:	8				
	The n bus. $\frac{1}{2}$ be $\geq$ buses 128 b	nemory bus The data bu 32 bits wid tend to bu its for data	s usually co us may be le. With t ecome incr and 44 bi	nsist of one 64 bits wid he introdu easingly w ts for addre	e address b e and the a ction of 64 ider. The esses.	us and one ddress bus -bit compu Itanium 2	data may iters, uses
	Opera A mo buses	ations in th dern CPU are usually	e compute may run a y a few (4-)	r are synch at a few GI 5) times slo	ronized by Hz (clock fr ower.	a clock. requency).	The
57				58			
A few words on 64-bit systems	CISC Each	(Complex instruction	Instruction can perfo	n Set Comj rm several	puters) bef low-level o	fore $\approx 1985$	such
<ul> <li>A larger address range, can address more memory.</li> <li>With 32 bits we can (directly) address 4 Gbyte, which is</li> </ul>	as a load from memory, an arithmetic operation, and a memory store, all in a single instruction.						
rather limited for some applications.	Why CISC?						
• Wider busses, increased memory bandwidth.	Advanced instructions simplified programming						
• 64-bit integers.	• Advanced instructions simplified programming (writing compilers, assembly language programming).						
Be careful when mixing binaries (object libraries) with your own code. Are the integers 4 or 8 bytes?	<ul><li>Software was expensive.</li><li>Memory was limited and slow so short programs were good.</li></ul>						
% cat kind.c #include <stdio.h></stdio.h>	(Complex instructions $\Rightarrow$ compact program.)						
int main()	C						
{	Some	drawbacks	:		1	-11-C	
<pre>printf("sizeof(short int) = %d\n", sizeof(short int)); printf("sizeof(int) = %d\n", sizeof(int));</pre>	• co	mplicated o	constructio	n could im	ply a lower	clock frequ	ency
<pre>printf("sizeof(long int) = %d\n", sizeof(long int));</pre>	• ins	struction p	ipelines ha	rd to imple	ement		
return 0.	• loi	ng design c	ycles				
}	• m	any design	errors				
<pre>% gcc kind.c On the student system % a.out sizeof(short int) = 2 sizeof(int) = 4 sizeof(long int) = 4</pre>	• on Ac av th pr	ly a small ccording to ailable 680: at approxi ogram requ	part of the Sun: Sun <sup>2</sup> 20-instruct mately 809 uires only 2	instructio s C-compil ions (Sun3 % of the c 20% of a p	ns was use er uses abo architectur omputation cocessor's i	d out 30% of ce). Studies ns for a ty nstruction	the s show pical set.
<pre>% a.out On another Opteron-system sizeof(short int) = 2</pre>	When memory became cheaper and faster, the decode and execution on the instructions became limiting.						
<pre>sizeof(int) = 4 sizeof(long int) = 8 4 if gcc -m32</pre>	Studie a simp one cy	es showed t ple instruct ycle.	hat it was p ion set and	possible to l where ins	improve pe tructions w	erformance vould execu	with ite in
59				60			

<ul> <li>RISC - Reduced Instruction Set Computer</li> <li>IBM 801, 1979 (publ. 1982)</li> <li>1980, David Patterson, Berkeley, RISC-I, RISC-II</li> <li>1981, John Hennessy, Stanford, MIPS</li> <li>≈ 1986, commercial processors</li> </ul>					Set ·I, RI	Co ISC-1	mput	Advantages: Simple design, easier to debug, cheaper to produce, shorter design cycles, faster execution, easier to write optimizing compilers (easier to optimize many simple instructions than a few complicated with dependencies between each other).				
<ul> <li>         ■ ≈ 1986, comm     </li> <li>A processor whose sequence of simple a large variety of</li> </ul>	<ul> <li>≈ 1986, commercial processors</li> <li>A processor whose design is based on the rapid execution of a sequence of simple instructions rather than on the provision of a large variety of complex instructions.</li> </ul>					rapio 1 on	l exe the j	ecution o provision	CISC - short programs using complex instructions. RISC - longer programs using simple instructions.			
Some RISC-chara	acterist	ics:								So why is RISC faster?		
• load/store arc	hitectu A	ire; C	! = A	4 H	3					The simplicity and uniformity of the instructions make it possible to use pipelining, a higher clock frequency and to write optimizing compilers.		
ADD R1, H	3 R2,R3									Will now look at some techniques used in all RISC-computers:		
STORE C,R: • fixed-format in bit positions i long)	3 nstruct in each	ions i inst	(the tructi	op-c ion v	ode i vhich	s alw is a	ays i lway	in the sa s one w	ame ord	<ul> <li>instruction pipelining work on the fetching, execution etc. of instructions in parallel</li> <li>cache memories small and fast memories between the main memory and the</li> </ul>		
• a (large) home be used in any	ogeneo z conte	us re xt ar	egiste 1d sir	r set nnlif	;, allo ving	wing	; any siler	register design	r to	CPU registers		
• simple address by sequences of	sing mo of simp	odes v ole ar	with ithm	more etic	e con instr	iplex uction	mod ns	les repla	iced	• superscalar execution parallel execution of instructions (e.g. two integer operations, *, + floating point)		
• one instruction	n/cycle	e										
• hardwired inst	tructio	ns an	nd no	t mi	croco	ode				The most widely-used type of microprocessor, the x86 (Intel), is		
<ul> <li>efficient pipeli</li> <li>simple FPUs; sin, exp etc. a</li> </ul>	ning only + ire don	•, -, * e in s	°, / a softw	nd v are.	/					CISC rather than RISC, although the internal design of newer x86 family members is said to be RISC-like. All modern CPUs share some RISC characteristics, although the details may differ substantially.		
			61							62		
Pipelining	- pe	rfor	miı	ng a	a ta	sk i	in s	evera	1	So one instruction completed per cycle once the pipeline is filled.		
Pipelining Analogy: building	- pe s g cars 1	rfor tep	rmii s, s an a	ng a tag	a ta es	sk i	n s	evera	1	So one instruction completed per cycle once the pipeline is filled. Not so simple in real life: different kind of <u>hazards</u> , that pre- vent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).		
Pipelining Analogy: building Suppose there are	- pe s g cars u e five s	rfor tep <sup>1sing</sup>	rmin s, s an a ; (can	ng a tag ssem	a ta es Ibly l more	sk i ine in ), .e.;	in s nafa	evera	1	So one instruction completed per cycle once the pipeline is filled. Not so simple in real life: different kind of <u>hazards</u> , that pre- vent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute, M, WM Memory	- pe s cars u e five s e next ion dec	rfor tep using tages instr ode. , wri	rmin S, S an a (can ructio te to	ng a tag ssem 1 be : on fro regi	a ta es Ibly 1 more om m	ine in ), .e.p nemor	n a fa g ry.	evera	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles for example)</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute M, WM Memory	- pe s g cars u e five s e next ion dec	rfor tep 1sing tages instr ode. , wri	rmin s, s an a (can uctio te to	ng : tag ssem 1 be : on fro regi	a ta es bbly l more om n sters	sk i ine in ), .e.; iemor	n s n a fa g ry.	evera	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li><u>Data hazards</u> arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory	- pe s g cars u e five s e next ion dec access	rfor tep sing tages instr ode. , wri	an a (can uctio te to <b>cycle</b>	ng : tag 1 be : n be : regi	a ta es bly l more om n sters ber	sk i ine in ), .e., iemor	in s 1 a fa g ry.	evera	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li><u>Data hazards</u> arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory	- pe s g cars u e five s e next ion dec access	rfor tep using tages instr ode. , wri Clock 3	rmin s, s an a (can ructio te to cycle 4	ng a tag ssem 1 be : on fro regi regi	a ta es ubly l more om n sters uber 6	sk i ine in ), .e.; aemor	in s nafa g ry. 8	evera actory.	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li><u>Data hazards</u> arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory	- pe s g cars u e five s e next ion dec access ( 2 <b>D</b>	rfor tep Ising tages instr ode. , wri Clock 3 EX	rmin s, s an a ; (can uctio te to cycle 4 M	ng a tag ssem 1 be : regi regi 5 WB	a ta es ubly l more om n sters uber 6	sk j ine in ), .e.j nemor	n s nafa g ry. 8	evera actory.	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li><u>Data hazards</u> arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory Instruction 1 k IF k+1	- pe s g cars u e five s e next ion dec access ( 2 ID IF	rfor tep sing tages instr ode. , wri Clock 3 EX ID	rmin s, s an a s (can ructio te to cycle 4 M EX	ng a tag ssem n be regi regi 5 WB M	a ta es ubly l more om n sters ber 6 WB	sk i ine in ), .e.; aemor	in s nafa g ry. 8	evera actory.	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li><u>Data hazards</u> arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> <li>The second addition must not start until a is available.</li> <li><u>Control hazards</u> arise from the pipelining of branches (if statemente)</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory Instruction 1 k IF k+1 k+2	- pe s g cars u e five s e next ion dec access ( 2 ID IF	rfor tep Ising tages instr ode. , wri Clock 3 EX ID IF	rmin s, s an a ; (can uctio te to cycle 4 M EX ID	ng a tag ssem i be : on fro regi : num 5 WB M EX	a ta es ubly l more om m sters ber 6 WB M	sk j ine in ), .e.j iemor	n s n a fa g ry. 8	evera actory.	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li><u>Data hazards</u> arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> <li>The second addition must not start until a is available.</li> <li><u>Control hazards</u> arise from the pipelining of branches (if-statements).</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory Instruction 1 k IF k+1 k+2 k+3	- pe s cars u e five s e next ion dec access ( 2 ID IF	rfor tep sing tages instr ode. , wri Clock 3 EX ID IF	rmin s, s an a ; (can ructio te to cycle 4 M EX ID	ng a tag ssem i be : on fro regi s num 5 WB M EX	a ta es ably l more om n sters ber 6 WB M FX	sk i ine in ), .e. nemor 7 7 WB	n s n a fa g ry. 8	evera actory.	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li><u>Structural hazards</u> arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li><u>Data hazards</u> arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> <li>The second addition must not start until a is available.</li> <li><u>Control hazards</u> arise from the pipelining of branches (if-statements).</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory Instruction 1 k IF k+1 k+2 k+3 b:4	- pe s g cars u e five s e next ion dec access ( 2 ID IF	rfor tep sing tages instr ode. , wri Clock 3 EX ID IF	rmin s, s, s an a ; (can uctio te to cycle 4 M EX ID IF	ng a tag sssem i be : on fro regi : num 5 WB M EX ID	a ta es ubly l more om n sters ber 6 WB M EX	sk j ine in ), .e., iemor 7 WB M	in s g ry. 8 WB	evera actory.	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li>Structural hazards arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li>Data hazards arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> <li>The second addition must not start until a is available.</li> <li>Control hazards arise from the pipelining of branches (if-statements).</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory Instruction 1 k IF k+1 k+2 k+3 k+4	- pe s cars u e five s e next ion dec access ( 2 ID IF	rfor tep sing tages instr ode. , wri Clock 3 EX ID IF	rmin s, s an a ; (can ructio te to cycle 4 M EX ID IF	ng a tag ssem i be i on fro regi s num 5 WB M EX ID IF	a ta es ably l more om n sters ber 6 WB M EX ID	sk i ine in ), .e. nemor 7 WB M EX	in s g ry. 8 WB M	evera actory. 9	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li>Structural hazards arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li>Data hazards arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> <li>The second addition must not start until a is available.</li> <li>Control hazards arise from the pipelining of branches (if-statements).</li> </ul>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory Instruction 1 k IF k+1 k+2 k+3 k+4	- pe s cars u e five s e next ion dec access ( 2 ID IF	rfor tep sing tages instr ode. , wri Clock 3 EX ID IF	rmin s, s; s an a ; (can uctio te to cycle 4 M EX ID IF	ng a tag ssem i be i on fro regi s num 5 WB M EX ID IF	a ta es ubly l more om n sters sters 6 WB M EX ID	sk j ine in ), .e. nemor 7 7 WB M EX	in s g ry. 8 WB M	evera actory. 9 WB	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li>Structural hazards arise from resource conflicts, e.g. <ul> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> </ul> </li> <li>Data hazards arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g. <ul> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> </ul> </li> <li>The second addition must not start until a is available.</li> <li>Control hazards arise from the pipelining of branches (if-statements).</li> </ul> <li>An example of a control hazard: <ul> <li>if (a &gt; b - c * d) then do something else do something else and if</li> </ul> </li>		
Pipelining Analogy: building Suppose there are IF Fetch th ID Instructi EX Execute. M, WM Memory Istruction 1 k IF k+1 k+2 k+3 k+4	- pe s g cars u e five s e next access ( 2 ID IF	rfor tep sing tages instr ode. , wri Clock 3 EX ID IF	rmin s, s, s an a c (can uctio te to cycle 4 M EX ID IF	ng a tag ssem n be : on fro regi : num 5 WB M EX ID IF	a ta es ubly l more om n sters sters 6 WB M EX ID	sk j ine in ), .e., iemor 7 WB M EX	in s g ry. 8 WB M	evera actory. 9 WB	1	<ul> <li>So one instruction completed per cycle once the pipeline is filled.</li> <li>Not so simple in real life: different kind of <u>hazards</u>, that prevent the next instruction from executing during its designated clock cycle. Can make it necessary to stall the pipeline (wait cycles).</li> <li>Structural hazards arise from resource conflicts, e.g.</li> <li>two instructions need to access the system bus (fetch data, fetch instruction),</li> <li>not fully pipelined functional units (division usually takes 10-20 cycles, for example).</li> <li>Data hazards arise when an instruction depends on the results of a previous instruction (will look at some cases in later lectures) e.g.</li> <li>a = b + c</li> <li>d = a + e</li> <li>d depends on a</li> <li>The second addition must not start until a is available.</li> <li>Control hazards arise from the pipelining of branches (if-statements).</li> </ul> An example of a control hazard: <ul> <li>if (a &gt; b - c * d) then</li> <li>do something else</li> <li>end if</li> </ul> Must wait for the evaluation of the logical expression.		
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Several techniques to minimize hazards (look in the literature for details) instead of just stalling. Some examples: • Add hardware; can compute the address of the branch target Structural hazard: or not. Add hardware. If the memory has only one port LOAD adr,R1 will stall the pipeline (the fetch of data will conflict with a later instruction fetch). Add a memory port (separate data and instruction caches). times but the last. Data hazards: • Forwarding: **b** + **c** available after EX, special hardware we should branch or not. "forwards" the result to the a + e computation (without involving the CPU-registers). • Instruction scheduling. The compiler can try and rearrange the order of instruction to minimize stalls. Try to change the order between instructions using the waittime to do something useful. Perform the FADD-instruction while waiting for the if to complete. a = b + cd = a + eload b the branch is taken, must be able do undo. load c add b + c has to wait for load c to complete load b load c give the load c time to complete load e add b + c in parallel with load e

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### Superscalar CPUs

Fetch, decode and execute more than one instruction in parallel. More than one finished instruction per clock cycle. There may, e.g. be two integer ALUs, one unit for floating point addition and subtraction one for floating point multiplication. The units for +, - and \* are usually piplined (they need several clock cycles to execute).

There are also units for floating point division and square root; these units are not (usually) pipelined.

MULT XXXXXXX MULT XXXXXXXX MULT \*\*\*\*\*\*

Compare division; each xxxxxxxx is 22 cycles (on Sun):

DIV	XXXXXXXXXX
DIV	xxxxxxxxx
DIV	*****

How can the CPU keep the different units busy? The CPU can have circuits for arranging the instructions in suitable order, dynamic scheduling (out-of-order-execution).

To reduce the amount of hardware in the CPU we can let the compiler decide a suitable order. Groups of instructions (that can be executed in parallel) are put together in packages. The CPU fetches a whole package and not individual instructions. VLIW-architecture, Very Long Instruction Word.

The Intel & HP Itanium CPU uses VLIW (plus RISC ideas). Read the free chapter from: W. Triebel, Itanium Architecture for Software Developers. See the first chapter in: IA-32 Intel Architecture Optimization Reference Manual for details aboute the Pentium 4. Read Appendix A in the Software Optimization Guide for AMD64 Processors. See the web-Diary for links.

#### Control hazards: (many tricks)

- earlier and can decide whether the branch should be taken
- Branch prediction; try to predict, using "statistics", the way a branch will go. Compile-time/run-time. Can work very well. The branch att the end of a for-loops is taken all the
- Branch delay slot: let the compiler rearrange instructions so that something useful can be done while it is decided whether

loop:	instr	loop:	instr
	instr		instr
	•••	>	•••
	FADD R1, R2, R3		if j < n goto loop
	if j < n goto loop		FADD R1, R2, R3

A more general construction, speculative execution: Assume the branch not taken and continue executing (no stall). If

More on parallel on floating point operations.

flop = floating point operation.flops = plural of flop  $\underline{or}$  flop / second.

In numerical analysis a flop may be an addition-multiplication pair. Not unreasonable since (+, \*) often come in pairs, e.g. in an inner product.

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Top floating point speed =# of processors  $\times$  flop / s = # of processors  $\times$  # flop / clock cycle  $\times$  clock frequency

Top performance for some CPUs. I have used (double precision):

CPU	+  or $*$	clock f.	top speed
	per cycle	GHz	Gflops
IBM RS6000	4	0.16	0.64
Itanium 2	4	0.9	3.6
AMD Opteron	$^{2}$	<b>2</b>	4
AMD64	<b>2</b>	$^{2}$	4
Pentium 4	1	<b>2</b>	$^{2}$

Some Intel, AMD and Motorola CPUs have another unit (a kind of vector unit) that can work on short vectors of numbers. These technologies have names like: SSE3, 3DNow! and AltiVec. More details later in the course.

To use the the vector unit you need a compiler that can vectorize. The vector unit may not be IEEE 754 compliant (not correctly rounded). So results may differ between the vectorized and unvectorized versions of the same code. See www.spec.org for benchmarks with real applications.

Why do we often only get a small percentage of these speeds? Is it possible to reach the top speed (and how)?



Addition and multiplication are pipelined. Division is not pipelined (so divides do not overlap) and takes 22 cycles for double precision.

$$rac{167\cdot 10^6 s^{-1}}{22}pprox 7.6\cdot 10^6/s$$

So, the answer is sometimes

- provided we have a suitable instruction mix and that
- we do not access memory too often

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## Memory is the problem - caches





CPU: increase 1.35 improvement/year until 1986, and a 1.55 improvement/year thereafter.

DRAM (dynamic random access memory), slow and cheap, 1.07 improvement/year.

Use SRAM (static random access memory) fast & expensive for cache.

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There are more general cache constructions. This is a two-way set associative cache:



A direct mapped cache is one-way set associative.

In a fully associative cache data can be placed anywhere.



Direct mapped cache Cache CPU

I/O devices

The cache is a small and fast memory used for storing both instructions and data.

Memory

This is the simplest form of cache-construction.

Cache Main memory variable, e.g. 4 bytes 0 these lines occupy the the same place cache line in the cache copy the whole line even if only a few bytes are needed 71

To use a cache efficiently locality is important.

• instructions: small loops, for example

• data: use part of a matrix (blocking)

# Main memory





L1 and L2 caches

Not necessarily good locality  $\underline{together}$ .

Make separate caches for data and instructions.

Can read instructions and data in parallel.

Memory hierarchy.

Faster

Newer machines even have an L3 cache.

# The AMD64 (student machines)

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(Some) Intel and AMD-CPUs have an instruction, cpuid, that gives details about the CPU, such as model, SSE-features, L1- and L2-cache properties. These values can be hard to find just reading manuals. Some parameters are available in /proc/cpuinfo .

Unfortunately one has to code in assembler to access this information. gcc supports inlining of assembly code using the asm-function. asm makes it possible to "connect" registers with C-variables. It may look like this (note that I have broken the string):

```
. . .
unsigned long before, after;
/* Does the CPU support the cpuid-instruction? */
asm("pushfl; popl %%eax; movl %%eax, %0;
     xorl $0x40000, %%eax; pushl %%eax; popfl; pushfl;
     popl %%eax; movl %%eax, %1; pushl %0; popfl "
     : "=r" (before), "=r" (after)
                                     /* output */
                                      /* input */
      :
        "eax"
                          /* changed registers */
     :
    );
if ( before != after ) {
                         /* Support. Test more */
}
```

One can call cpuid with a set of different "arguments", and cpuid then returns bit patterns in four registers. Reading the AMD-manual "CPUID Specification" one can interpret the bits. Bits 31-24 in the ECX-register contain the size of L1-data cache in kbyte, for example. This is some of the facts I found out about the caches (I read some manuals as well):

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The L1 data cache is 64 kbyte, 2-way associative and has a cache line size (length) of 64 bytes. Cache-line replacement is based on a least-recently-used (LRU) replacement algorithm.

The L2 cache is "on-die" (on-chip), 512 kbyte and 16-way associative. The cache line size is 64 bytes.

#### A note on reading assembly output

In the lecture and during the labs I said it was sometimes useful to look at the assembler code produced by the compiler. Here comes a simple example. Let us look at the the following function.

```
double dot(double x[], double y[], int n)
{
    double s;
    int k;
    s = 0.0;
    for (k = 0; k < n; k++)
        s += x[k] * y[k];
    return s;</pre>
```

}

First some typical RISC-code from a Sun ULTRA-Sparc CPU. I used gcc and compiled the code by:

gcc -S -O3 dot.c

-S produces the assembler output on dot.s. Here is the loop (code for passing parameters, setting up for the loop, and returning the result is not included).

.LL5:		My translation
ldd	[%o0+%g1], %f8	f8 = x[k]
ldd	[%o1+%g1], %f10	f10 = y[k]
add	%g2, 1, %g2	k = k + 1
fmuld	%f8, %f10, %f8	%f8 = %f8 * %f10
cmp	%o2, %g2	k == n? Set status reg.
faddd	%f0, %f8, %f0	%f0 = %f0 + %f8
bne	.LL5	if not equal, go to .LL5
add	%g1, 8, %g1	increase offset

When the loop is entered **%ebx** and **%ecx** contain the addresses of the first elements of the arrays. Zero has been pushed on the stack as well (corresponds to s = 0.0).

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fldl (%ebx,%eax,8) loads a 64 bit floating point number. The
address is given by %ebx + %eax\*8. The number is pushed on
the top of the stack, given by the stackpointer %st.

Unlike the Sparc, the AMD can multiply with an operand in memory (the number does not have to be fetched first). So the fmull multiplies the top-element on the stack with the number at address %ecx + %eax\*8 and replaces the top-element with the product.

faddp %st, %st(1) adds the top-elements on the stack
(the product and the sum, s), pops the stack, the p in faddp,
and replaces the top with the new value of s.

incl increases k (stored in %eax) and cmpl compares it to n. jne stands for jump if not equal.

Some comments.

f and f are registers in the FPU. When entering the function, the addresses of the first elements in the arrays are stored in registers 00 and 01. The addresses of x[k] and y[k] are given by 00 + 8k and 1 + 8k. The reason for the factor eight is that the memory is byte addressable (each byte has an address). The offset, 8k, is stored in register g1.

The offset, 8k, is updated in the last add. It looks a bit strange that the add comes after the branch, bne. The add-instruction is, however, placed in the branch delay slot of the branch-instruction, so it is executed in parallel with the branch.

add is an integer add. faddd is a "floating point add double". It updates f0, which stores the sum. f0 is set to zero before the loop. cmp compares k with n (the last index) by subtracting the numbers. The result of the compare updates the Z-bit (Z for zero) in the integer condition code register. The branch instruction looks at the Z-bit to see if the branch should be taken or not.

We can make an interesting comparison with code produced on the AMD64. The AMD (Intel-like) has both CISC- and RISCcharacteristics. It has fewer registers than the Sparc and it does not use load/store in the same way. The x87 (the FPU) uses a stack with eight registers. In the code below, **eax** etc. are names of 32-bit CPU-registers. (in the assembly language a % is added).

```
.L5:

fldl (%ebx,%eax,8)

fmull (%ecx,%eax,8)

faddp %st, %st(1)

incl %eax

cmpl %eax, %edx

jne .L5
```

#### Virtual memory

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Use disk to "simulate" a larger memory. The virtual address space is divided into <u>pages</u> e.g. 4 kbytes. A virtual address is translated to the corresponding physical address by hardware and software; address translation.



A page is copied from disk to memory when an attempt is made to access it and it is not already present (page fault). When the main memory is full, pages must be stored on disk (e.g. the least recently used page since the previous page fault). Paging. (Swapping; moving entire processes between disk and memory.)

Some advantages of virtual memory:

- simplifies relocation (loading programs to memory), independece of physical addresses; several programs may reside in memory
- security, can check access to protected pages, e.g. read-only data; can protect data belonging to other processes
- allows large programs to run on little memory; only used sections of programs need be present in memory; simplifies programming (e.g. large data structures where only a part is used)

Virtual memory requires  $\underline{locality}$  (re-use of pages) to work well, or thrashing may occur.

#### A few words on address translation

The following lines sketch one common address translating technique.

A virtual address is made up by two parts, the virtual page number and the page offset (the address from the top of the page).

The page number is an index into a page table:

```
physical page address =
    page_table(virtual page number)
```

The page table is stored in main memory (and is sometimes paged). To speed up the translation (accessing main memory takes time) we store part of the table in a cache, a translation lookaside buffer, TLB which resides in the CPU ( $\mathcal{O}(10) - \mathcal{O}(1000)$  entries).

Once again we see that locality is important. If we can keep the references to a few pages, the physical addresses can found in the TLB and we avoid a reference to main memory. If the address is not available in the TLB we get a TLB miss (which is fairly costly, taking tens of clock cycles).

Reading the actual data may require a reference to main memory, but we hope the data resides in the L1 cache.

Second best is the L2 cache, but we may have to make an access to main memory, or worse, we get a page fault and have to make a disk access (taking millions of clock cycles).

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### Your situation

• A large and old code which has to be optimized. Even a slight speedup would be of use, since the code may be run on a daily basis.

• A new project, where language and data structures have to be chosen.

 $C \approx 2$  Fortran,  $C++ \approx 4$  Fortran (for floating point). Java? Can be slow and use large amounts of memory. See the article (Springer chapter) for an example.

Should it be parallel?

Test a simplified version of the computational kernel. For tran for floating point,  $\rm C/C++$  for the rest.

• Things that are done once. Let the computer work. Unix-tools, Matlab, Maple, Mathematica ...

## **Code Optimization**

- How does one get good performance from a computer system?
- Focus on systems with one CPU and floating point performance.
- To get maximum performance from a parallel code it is important to tune the code running on each CPU.
- Not much about applications from graphics, audio or video. One example of SSE2 (Streaming SIMD Extensions 2).
- General advice and not specific systems.
- Fortran, some C (hardly any C++). Some Java in the Springer chapter.

More about unix-tools:

- shell scripts (sh, csh, tcsh, ksh, bash) (for, if, | pipes and lots more)
- awk (developed by Alfred Aho, Peter Weinberger, and Brian Kernighan in 1978)

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- sed (stream editor)
- grep (after the qed/ed editor subcommand "g/re/p", where re stands for a regular expression, to Globally search for the Regular Expression and Print)
- tr (translate characters)
- perl (Larry Wall in 1987; contains the above)
- etc.

Some very simple examples:

Counting the number of lines in a file(s):

%	wc	file	or	wc	-1	file
%	wc	files	or	wc	-1	files

Finding a file containing a certain string

%	grep	string files	e.g.
%	grep	'program matrix' *.f90	or
%	grep	-i 'program matrix' *.f90	etc.

The grep-command takes many flags.

Example, interchange the two blank experied columns of	Just the other day (two years and)
numbers in a file:	Just the other day (two years ago)
% awk '{print \$2, \$1}' file	You have $\approx 600$ files each consisting of $\approx 24000$ lines (a total of $\approx 14 \cdot 10^6$ lines) essentially built up by:
<pre>Example: sum the second columns of a set of datatfiles. Each row contains: number number text text The files are named data.01, data.02, foreach? is the prompt. % foreach f ( data.[0-9][0-9] ) foreach? echo -n \$f': ' foreach? echo -n \$f': ' foreach? end data.01: 30 data.02: 60 data.03: 77 data.20: 84 Another possibility is: awk '{s += \$2} END {print FILENAME ": " s}' \$f</pre>	<pre><doc> <text> Many lines of text (containing no DOC or TEXT) </text> </doc> <doc> <text> Many lines of text </text> </doc> etc. There is a mismatch between the number of DOC and TEXT. Find it! We can localize the file this way: % foreach f ( * ) foreach? if ( 'grep -c "<doc>" \$f` != \</doc></pre>
85	86
The optimization process Basic: Use an efficient algorithm. Simple things: • Use (some of) the optimization options of the compiler. Optimization can give large speedups (and new bugs, or reveal bugs). Read the manual page for your compiler. Even better, read the tuning manual for the system. • Switch compiler and/or system.	<ul> <li>The next page lists the compiler options of the Sun Fortran90/95-compiler. The names are not standardized, but it is common that -c means "compile only, do not link". To produce debug information -g is used.</li> <li>-O[n] usually denotes optimization on level n. There may be an option, like -fast, that gives a combination of suitable optimization options. In Sun's case -fast is equivalent to: <ul> <li>-xtarget=native optimize for host system (sets cache sizes for example).</li> <li>-05 highest optimization level.</li> <li>-1ibmil inline certain math library routines.</li> <li>-fsimple=2 aggressive floating-point optimizations. May cause many programs to produce different numeric results due to changes in rounding.</li> <li>-dalign align data to allow generation of faster double word load/store instructions.</li> <li>-xlibmopt link the optimized math library. May produce slightly different results; if so, they usually differ in the last bit.</li> <li>-depend optimize DO loops better.</li> </ul> </li> </ul>

```
If you are willing to work more...
f95 | f90 [ -a ] [ -aligncommon[=a] ] [ -ansi ]
 [ -autopar ] [ -Bx ] [ -C ] [ -c ] [ -cg89 ] [ -cg92 ]
 [ -copyargs ] [ -Dnm[=def] ] [ -dalign ] [ -db ]
   -dbl_align_all[=yes no] ] [ -depend ] [ -dryrun ]
 Γ
                                                                • Decrease number of disk accesses (I/O, virtual memory)
 [ -d[y|n] ] [ -e ] [ -erroff=taglist ] [ -errtags[=yes|r
 [ -explicitpar ] [ -ext_names=e ] [ -F ] [ -f ]
                                                                • (LINPACK, EISPACK) \rightarrow LAPACK
 [ -fast ] [ -fixed ] [ -flags ] [ -fnonstd ]
                                                                • Use numerical libraries tuned for the specific system, BLAS
   -fns=yes|no] [ -fpover=yes|no ] [ -fpp ] [ -free ]
 E
 [ -fround=r ] [ -fsimple[=n] ] [ -ftrap=t ] [ -G ]
 [ -g ] [ -hnm ] [ -help ] [ -Idir ] [ -inline=rl ]
                                                               Find bottlenecks in the code (profilers).
 [ -Kpic ] [ -KPIC ] [ -Ldir ] [ -libmil ] [ -loopinfo ]
 E
   -M dir ] [ -mp=x ] [ -mt ] [ -native ] [ -noautopar ]
                                                               Attack the subprograms taking most of the time.
 [ -nodepend ] [ -noexplicitpar ] [ -nolib ] [ -nolibmil
                                                               Find and tune the important loops.
 [ -noqueue ] [ -noreduction ] [ -norunpath ] [ -0[n] ]
 [ -o nm ] [ -onetrip ] [ -openmp ] [ -p ] [ -pad[=p] ]
                                                               Tuning loops has several disadvantages:
   -parallel] [ -pg ] [ -pic ] [ -PIC ] [ -Qoption pr ls
 Г
                                                                 • The code becomes less readable and it is easy to introduce
 [ -qp ] [ -R list ] [ -r8const ] [ -reduction ] [ -S ]
                                                                  bugs.
 [ -s ] [ -sb ] [ -sbfast ] [ -silent ] [ -stackvar ]
 [ -stop_status=yes no ] [ -temp=dir ] [ -time ] [ -U ]
                                                                • Detailed knowledge about the system, such as cache
 [ -Uname ] [ -u ] [ -unroll=n ] [ -V ] [ -v ] [ -vpara
                                                                  configuration, is often necessary.
 [ -w ] [ -xa ] [ -xarch=a ] [ -xautopar ] [ -xcache=c ]
                                                                 • What is optimal for one system need not be optimal for
 [ -xcg89 ] [ -xcg92 ] [ -xchip=c ] [ -xcode=v ]
                                                                  another; faster on one machine may actually be slower on
 [ -xcommonchk[=no yes] ] [ -xcrossfile=n ] [ -xdepend ]
                                                                  another.
 [-xexplicitpar][-xF][-xhasc[=yes|no]][-xhelp=h
                                                                  This leads to problems with portability.
 [ -xia[=i] ] [ -xildoff ] [ -xildon ] [ -xinline=rl ]
 [ -xinterval=i ] [ -xipo[=0|1] ] [ -xlang=language[,lang
                                                                • Code tuning is not a very deterministic business.
 E
   -xlibmil ] [ -xlibmopt ] [ -xlicinfo ]
                                                                  The combination of tuning and the optimization done by the
 [ -xlic_lib=sunperf ] [ -Xlist ] [ -xloopinfo ] [ -xmaxe
                                                                  compiler may give an unexpected result.
 [ -xmemalign[=ab] ] [ -xnolib ] [ -xnolibmil ] [ -xnolib
                                                                • The computing environment is not static; compilers become
 [ -xO[n] ] [ -xopenmp ] [ -xpad ] [ -xparallel ] [ -xpg
                                                                  better and there will be faster hardware of a different
   -xpp=p ] [ -xprefetch=a[,a]] [ -xprofile=p ] [ -xrecum
 Γ
                                                                  construction.
 [ -xreduction ] [ -xregs=r ] [ -xs ] [ -xsafe=mem ]
                                                                  The new system may require different (or no) tuning.
   -xsb ] [ -xsbfast ] [ -xspace ] [ -xtarget=t ] [ -xtin
 E
 [ -xtypemap=spec ] [ -xunroll=n ] [ -xvector=yes | no ] [
   source file(s) ... [ -lx ]
                                                                                           90
What should one do with the critical loops?
                                                               What can you hope for?
The goal of the tuning effort is to keep the FPU(s) busy.
                                                                • Many compilers are good.
Accomplished by efficient use of
                                                                  May be hard to improve on their job.
 • memory hierarchy
                                                                  We may even slow the code down.
 • parallel capabilities
                                                                • Depends on code, language, compiler and hardware.
                                                                • Could introduce errors.
              Instruction
                                    Main
memory
   CPU
                         L2 cache
                                               Disks
                                                               But: can give significant speedups.
              L1 caches
                                                               Not very deterministic, in other words.
                                                               Do not rewrite all the loops in your code.
              Data
           Size
```

Superscalar: start several instructions per cycle. Pipelining: work on an instruction in parallel.

Locality of reference, data reuse

Avoid data dependencies and other constructions that give pipeline stalls

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Speed

### Choice of language

Fortran, C/C++ dominating languages for high performance numerical computation. There are excellent Fortran compilers due to the competition

between manufacturers and the design of the language. It may be harder to generate fast code from C/C++ and it is easy to write inefficient programs in C++

n, was chosen such that the three vectors would fit in the L1-cache, all at the same time.

On the two systems tested (in 2005) the Fortran routine was  $\ensuremath{\mathsf{twice}}$  as fast.

From the Fortran 90 standard (section 12.5.2.9):

"Note that if there is a partial or complete overlap between the actual arguments associated with two different dummy arguments of the same procedure, the overlapped portions must not be defined, redefined, or become undefined during the execution of the procedure."

Not so in C. Two pointer-variables with different names may refer to the same array.

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If that is the loop you need (in Fortran) write:

do k = 1, n - 1 c(k + 1) = a(k) + f \* c(k)end do

This loop is slower than the first one (slower in C as well).

In C, aliased pointers and arrays are allowed which means that it may be harder for a C-compiler to produce efficient code. The C99 **restrict** type qualifier can be used to inform the compiler that aliasing does not occur.

It is not supported by all compilers and even if it is supported it may not have any effect (you may need a special compiler flag, e.g. -std=c99).

An alternative is to use compiler flags, -fno-alias, -xrestrict etc. supported by <u>some</u> compilers. If you "lie" (or use a Fortran routine with aliasing) you may get the wrong answer!

The compilers on Lucidor (Itanium 2 at PDC) have improved since 2005, so restrict or -fno-alias are not needed (for add). Restricted pointers give a slight improvement on Lenngren (Intel Xeon, PDC) from 2s to 1.5s ( $10^5$  calls of add with n = 10000).

So this is not a static situation. Compilers and hardware improve every year, so to see the effects of aliasing one may need more complicated examples than **add**. I have kept it because it is easy to understand. On the next page is a slightly more complicated example, but still only a few lines of code, i.e. far from a real code. A Fortran compiler may produce code that works on several iterations in parallel.

c(1) = a(1) + f \* b(1) c(2) = a(2) + f \* b(2) ! independent

Can use the pipelining in functional units for addition and multiplication.

The assembly code is often <u>unrolled</u> this way as well. The corresponding C-code may look like:

```
/* This code assumes that n is a multiple of four */ for(k = 0; k < n; k += 4) {
```

```
c[k] = a[k] + f * b[k];
c[k+1] = a[k+1] + f * b[k+1];
c[k+2] = a[k+2] + f * b[k+2];
c[k+3] = a[k+3] + f * b[k+3];
```

A programmer may write code this way, as well. Unrolling gives:

- fewer branches (tests at the end of the loop)
- more instructions in the loop; a compiler can change the order of instructions and can use prefetching

If we make the following call in Fortran, (illegal in Fortran, legal in C), we have introduced a data dependency.

Here is a polynomial evaluation using Horner's method:

```
subroutine horner(px, x, coeff, n)
integer j, n
double precision px(n), x(n), coeff(0:4), xj
do j = 1, n
xj = x(j)
px(j) = coeff(0) + xj*(coeff(1) + xj*(coeff(2) &
+ xj*(coeff(3) + xj*coeff(4))))
end do
```

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end

On Lucidor the Fortran code takes 0.23s and the C-code 22.5s. (n = 1000 and calling the routine  $10^5$  times).

A hundred times slower, so not everything is better this year. I compiled using icc -O3 .... Lowering the optimization level to -O1 helped somewhat, it gave the time 2.6s (a factor of 10).

If -fno-alias is used,  $C \approx$  Fortran.

It is easy to fix the C-code without using -fno-alias

```
...
double xj, c0, c1, c2, c3, c4;
/* no aliasing with local variables */
c0 = coeff[0]; c1 = coeff[1]; c2 = coeff[2];
c3 = coeff[3]; c4 = coeff[4];
for (j = 0; j < n; j++) {
    xj = x[j];
    px[j] = c0 + xj*(c1 + xj*(c2 + xj*(c3 + xj*c4)));
}
...</pre>
```

There is no difference between C and Fortran on Lenngren (for the Horner-benchmark).

Now to Horner with complex numbers using Fortran (complex is built-in) and C++ (using "C-arrays" of complex<double>). I got the

following times (using Intel's compilers),

n = 1000 and calling the routine  $10^5$  times:

System, compiler	ifort -	03	icpc	-02	icpc	-03
Lucidor	C	).9		6.3	1	02.9
Lenngren	1	L.9		3.7		5.0
Opteron	2	2.1		28.5		28.5

The Portland group compilers, on Lenngren, took 2.2s (Fortran) and 14.1s (C++).

Here are some tests of the GNU-compilers on the same code.

System, compiler	g95 ·	-03	gfortran	-03	g++	-03
Lucidor		NA		$\mathbf{N}\mathbf{A}$		26.0
Lenngren		NA		$\mathbf{N}\mathbf{A}$		1.9
Opteron		2.6		1.9		3.5

The free Sun Studio-compilers for Linux (Opteron) take 1.9s (Fortran) and 9.9s (C++).

These times may not be representative, my experience is that the gcc-family of compilers produce slower code than Intel's.

The tables do show that is <u>important</u> to test different systems, compilers and compiler-options.

The behaviour in the above codes changes when **n** becomes very large. CPU-bound (the CPU limits the performance) versus Memory bound (the memory system limits the performance).

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### Basic arithmetic and elementary functions

- Common that the FPU can perform + and \* in parallel.
- a+b\*c can often be performed with one round-off, multiply-add MADD or FMA.
- Several FMAs in parallel on some machines.
- + and \* usually pipelined, so one sum and a product per clock cycle in the best of cases (not two sums or two products).
- / not usually pipelined and may require around twenty clock cycles.

## Floating point formats

Type	min	min	max	bits in	
	denormalized	normalized		mantissa	
IEEE 32 bit	$1.4\cdot10^{-45}$	$1.2\cdot10^{-38}$	$3.4\cdot10^{38}$	<b>24</b>	
IEEE 64 bit	$4.9\cdot10^{-324}$	$2.2\cdot10^{-308}$	$1.8\cdot10^{308}$	53	

- Using single- instead of double precision can give better performance. Fewer bytes must pass through the memory system.
- The arithmetic may not be done more quickly since several systems will use double precision for the computation regardless.

The efficiency of FPUs differ (this on a 2 GHz Opteron).

```
>> A = rand(1000); B = A;
>> tic; C = A * B; toc
Elapsed time is 0.780702 seconds.
```

```
>> A = 1e-320 * A;
>> tic; C = A * B; toc
Elapsed time is 43.227665 seconds.
```

For better performance one can sometimes replace a division by a multiplication.

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```
vector / scalar
```

vector \* (1.0 / scalar)

Integer multiplication and multiply-add are often slower than their floating point equivalents.

```
program int_vs_float
  integer, parameter :: n = 10000
  integer
                    :: k
  real, dimension(n) :: arr
  real
                     :: s = 0.0
  arr = 1
  do k = 1, 100000
   s = s + product(arr)
  end do
  print*, s
end program int_vs_float
% time a.out
 100000.0
5.36u 0.05s 0:05.58 96.9%
Change to:
  integer, dimension(n) :: arr
  integer
                       :: s = 0.0
% time a.out
 100000
44.15u 0.02s 0:44.33 99.6%
```

```
program ugly
Elementary functions
                                                                   double precision :: x = 2.5d1
                                                                   integer
Often coded in C, may reside in the libm-library.
                                                                                      :: k
                                                                   do k = 1, 17, 2
                                                                     print'(1p2e10.2)', x, sin(x)
 • argument reduction
                                                                     x = x * 1.0d2
                                                                   end do

    approximation

 • back transformation
                                                                 end program ugly
Can take a lot of time.
                                                                 % a.out
                                                                   2.50E+01 -1.32E-01
                                                                   2.50E+03 -6.50E-01
>> v = 0.1 * ones(1000, 1);
                                                                   2.50E+05 -9.96E-01
>> tic; for k = 1:1000, s = sin(v); end; toc
                                                                   2.50E+07 -4.67E-01
elapsed_time =
                                                                   2.50E+09 -9.92E-01
    0.8840
                                                                   2.50E+11 -1.64E-01
                                                                    2.50E+13 6.70E-01
>> v = 1e10 * ones(1000, 1);
                                                                   2.50E+15 7.45E-01
>> tic; for k = 1:1000, s = sin(v); end; toc
                                                                   2.50E+17 4.14E+07
                                                                                           <---
elapsed_time =
    9.2969
                                                                 Some compilers are more clever than others, which is shown on
                                                                 the next page.
                                                                 You should know that, unless x is an integer, v^x is computed
                                                                 using something like:
                                                                                v^x = e^{\log(v^x)} = e^{x\log v}, \hspace{0.2cm} 0 < v, x
                            101
                                                                                              102
subroutine power(vec, n)
                                                                 "The Mathematical Acceleration SubSystem" MASS (IBM).
  integer
                                     :: k, n
  double precision, dimension(n) :: vec
                                                                 High performance versions of some intrinsic Fortran functions.
                                                                 Sacrifices a small amount of accuracy (last bit).
  do k = 1, n
    vec(k) = vec(k)**1.5d0 ! so vec(k)^1.5
                                                                 There are also vector versions of some of the functions.
                                                                 Must link with special libraries (scalar-MASS, vector-MASS).
  end do
end
                                                                 program mass_test
                                                                   integer, parameter
                                                                                                      :: n = 10000
Times with n = 10000 and called 10000 on a 2 GHz AMD64.
                                                                   double precision, dimension(n) :: v, sinv
                                                                 . . .
                           power opt. power
                                                                     v = ...
           Compiler -03
                                                                     call vsin(sinv, v, n) ! vector-sin
            Intel
                           1.2
                                       1.2
                                                                  . . .
            g95
                            8.2
                                       1.6
                                                                 end
           gfortran
                            8.1
                                       1.6
                                                                 Performance depends on the type of function, range of
Looking at the assembly output from Intel's compiler:
                                                                 arguments and vector length (when using the vector library).
                                                                 Two examples (normalised times, n = 5000):
 . . .
                                    <---- NOTE
         fsart
                                    <---- NOTE
         fmulp
                    %st, %st(1)
 . . .
                                                                         Function default scalar MASS vector MASS
g95 and gfortran call pow (uses exp and log).
                                                                            \sin
                                                                                     4.9
                                                                                               3.5
                                                                                                             1
                                                                                               2.8
                                                                            exp
                                                                                     4.5
                                                                                                             1
In "opt. power" I have written the loop this way:
  do k = 1, n
    vec(k) = sqrt(vec(k)) * vec(k)
  end do
```

SSE2, Streaming SIMD Extensions 2	Eliminating constant expressions from loops
<pre>Some CPUs have built-in "vector computers". The Pentium 4 SSE2 can do e.g. vector multiplies: a = a .* b (using Matlab notation) where a and b contain 4 single precision or 2 double precision numbers. We need an optimizing compiler that produces code using the special vector instructions. For example: % ifc -vec_report3 -03 -tpp7 -xW files (15) vector dependence: assumed FLOW dependence loop was not vectorized (23) LOOP WAS VECTORIZED. ! A simple benchmark s = 0.0 do k = 1, 10000 s = s + x(k) * y(k) OR s = s + sin(x(k)) * cos(y(k)) end do</pre>	<pre>pi = 3.14159265358979d0 do k = 1, 1000000     x(k) = (2.0 * pi + 3.0) * y(k) ! eliminated end do do k = 1, 1000000     x(k) = exp(2.0) * y(k) ! probably eliminated end do do k = 1, 1000000     x(k) = my_func(2.0) * y(k) ! cannot be eliminated end do Should use PURE functions, my_func may have side-effects.</pre>
Called 100000 times. Times (in s) on a 2.8 GHz Intel Xeon: $\begin{array}{c c c c c c c c c c c c c c c c c c c $	
105	106
Virtual memory and paging	% vmstat 1 (edited)
• Simulate larger memory using disk.	page cpu
• Virtual memory is divided into pages, perhaps 4 or 8 kbyte	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$
Maxing pages between disk and physical memory is known	0 0 0 100
• Moving pages between disk and physical memory is known	352 128 0 0 100 < third test is run
as paging.	616 304 0 6 94
as paging. • Avoid excessive use. Disks are slow.	616 304 0 6 94 608 384 0 2 98
as paging. • Avoid excessive use. Disks are slow.	616       304       0       6       94         608       384       0       2       98         712       256       0       2       98       etc. for over 3 minutes
as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, $m * n^2$ is constant, so same number of additions	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, $m * n^2$ is constant, so same number of additions >> type test % list the program	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<ul> <li>as paging.</li> <li>Avoid excessive use. Disks are slow.</li> <li>This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions</li> <li>&gt; type test % list the program clear A B C % remove the matrices</li> </ul>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<ul> <li>as paging.</li> <li>Avoid excessive use. Disks are slow.</li> <li>This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions</li> <li>&gt; type test % list the program</li> <li>clear A B C % remove the matrices</li> <li>tic % start timer</li> <li>for k = 1:m % repeat m times</li> </ul>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<ul> <li>as paging.</li> <li>Avoid excessive use. Disks are slow.</li> <li>This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions</li> <li>&gt; type test % list the program clear A B C % remove the matrices tic % start timer for k = 1:m % repeat m times <pre>A = ones(n); % n x n-matrix of ones B = ones(n); % all are 64-bit numbers</pre></li></ul>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test</pre>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test</pre>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test</pre>	<pre>616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second</pre>
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test</pre>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test  % list the program clear A B C  % remove the matrices tic  % start timer for k = 1:m  % repeat m times A = ones(n);  % n x n-matrix of ones B = ones(n);  % all are 64-bit numbers C = A + B; end toc  % stop timer % Run three test cases &gt;&gt; n = 500; m = 16; test % 5.7 Mbyte for A, B and C elapsed time = 1 1287  % reughly ONE SECOND</pre>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test % list the program clear A B C % remove the matrices tic % start timer for k = 1:m % repeat m times A = ones(n); % n x n-matrix of ones B = ones(n); % all are 64-bit numbers C = A + B; end toc % stop timer % Run three test cases &gt;&gt; n = 500; m = 16; test % 5.7 Mbyte for A, B and C elapsed_time = 1.1287 % roughly ONE SECOND</pre>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test</pre>	<pre>616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second</pre>
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test % list the program clear A B C % remove the matrices tic % start timer for k = 1:m % repeat m times A = ones(n); % n x n-matrix of ones B = ones(n); % all are 64-bit numbers C = A + B; end toc % stop timer % Run three test cases &gt;&gt; n = 500; m = 16; test % 5.7 Mbyte for A, B and C elapsed_time = 1.1287 % roughly ONE SECOND &gt;&gt; n = 1000; m = 4; test % 22.9 Mbyte elapsed_time = 1.1234 % roughly the same as above &gt;&gt; n = 2000; m = 1; test % 91.6 Mbyte</pre>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test % list the program clear A B C % remove the matrices tic % start timer for k = 1:m % repeat m times A = ones(n); % n x n-matrix of ones B = ones(n); % all are 64-bit numbers C = A + B; end toc % stop timer % Run three test cases &gt;&gt; n = 500; m = 16; test % 5.7 Mbyte for A, B and C elapsed_time = 1.1287 % roughly ONE SECOND &gt;&gt; n = 1000; m = 4; test % 22.9 Mbyte elapsed_time = 1.1234 % roughly the same as above &gt;&gt; n = 2000; m = 1; test % 91.6 Mbyte elapsed_time = 187.9 % more than THREE MINUTES</pre>	616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test % list the program clear A B C % remove the matrices tic % start timer for k = 1:m % repeat m times A = ones(n); % n x n-matrix of ones B = ones(n); % all are 64-bit numbers C = A + B; end toc % stop timer % Run three test cases &gt;&gt; n = 500; m = 16; test % 5.7 Mbyte for A, B and C elapsed_time = 1.1287 % roughly ONE SECOND &gt;&gt; n = 1000; m = 4; test % 22.9 Mbyte elapsed_time = 1.1234 % roughly the same as above &gt;&gt; n = 2000; m = 1; test % 91.6 Mbyte elapsed_time = 187.9 % more than THREE MINUTES</pre>	<pre>616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second</pre>
<pre>as paging. • Avoid excessive use. Disks are slow. This test-program was run on a machine with only 64 Mbyte memory, m * n<sup>2</sup> is constant, so same number of additions &gt;&gt; type test % list the program clear A B C % remove the matrices tic % start timer for k = 1:m % repeat m times A = ones(n); % n x n-matrix of ones B = ones(n); % all are 64-bit numbers C = A + B; end toc % stop timer % Run three test cases &gt;&gt; n = 500; m = 16; test % 5.7 Mbyte for A, B and C elapsed_time = 1.1287 % roughly ONE SECOND &gt;&gt; n = 1000; m = 4; test % 22.9 Mbyte elapsed_time = 1.1234 % roughly the same as above &gt;&gt; n = 2000; m = 1; test % 91.6 Mbyte elapsed_time = 187.9 % more than THREE MINUTES</pre>	<pre>616 304 0 6 94 608 384 0 2 98 712 256 0 2 98 etc. for over 3 minutes pi = kilobytes paged in / second po = kilobytes paged out / second</pre>

### Input-output

Need to store  $5 \cdot 10^6$  double precision numbers in a file. A local disk was used for the tests. Intel's Fortran compiler on AMD64. Roughly the same times in C.

Test	Statement		time (s) size	(Mbyte)
1	write(10,	'(1pe23.16)') x(k)	29.4	114.4
<b>2</b>	write(10)	x(k)	19.5	76.3
3	write(10)	(vec(j), j = 1, 10000)	0.1	38.2
4	write(10)	vec(1:10000)	0.1	38.2
<b>5</b>	write(10)	vec	0.1	38.2

File sizes:

1: 
$$\underbrace{5 \cdot 10^6}_{\# \text{ of numbers}} \cdot \underbrace{(23+1)}_{\text{characters + newline}} / \underbrace{2^{20}}_{\text{Mbyte}} \approx 114.4$$

2: 
$$\underbrace{5 \cdot 10^6}_{\# \text{ of numbers}} \cdot \underbrace{(8+4+4)}_{\text{number + delims}} / \underbrace{2^{20}}_{\text{Mbyte}} \approx 76.3$$

$$3-5: \left\lfloor \underbrace{\underbrace{5\cdot10^6}_{\# \text{ of numbers}} \cdot \underbrace{8}_{\text{number}} +500 \cdot \underbrace{(4+4)}_{\text{delims}} \right\rfloor / \underbrace{2^{20}}_{\text{Mbyte}} \approx 38.2$$

In 5 vec has 10000 elements and we write the array 500 times.

g95 and gfortran were slower in all cases but case 2, where g95 took 6s.

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## Memory locality and caches



Search -->



## Portability of binary files?

- Perhaps
- File structure may differ
- Byte order may differ
- Big-endian, most significant byte has the lowest address ("big-end-first").
- The Intel processors are little-endian ("little-end-first").

On a big-endian machine write(10) -1.0d-300, -1.0d0, 0.0d0, 1.0d0, 1.0d300

```
Read on a little-endian
2.11238712E+125 3.04497598E-319 0.
3.03865194E-319 -1.35864115E-171
```

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#### Analysis

- Fortran stores matrices by columns
- (C stores matrices by rows)
- L1 data cache is two-way set-associative, two sets with 512 lines each (MIPS R10000, SGI)
- Replacement policy is LRU (Least Recently Used)
- One column per L1 cache line

 $\bullet$  When  $\leq 1024$  columns only cache misses in the first search

Suppose we have two sets of four cache lines, instead.

Assume we have nine columns.

sets			
1   5	9   5	5   1	5   9
12  6	2   6	2   6	2   6
3   7	3   7	3   7	3   7
4   8	4   8	4   8	4   8
after 8	after 9	after 8	after 9
cols	cols	next search	

Assume we have twelve columns.

first	search	I	next search		
1   5	9  5	9   1	5   1	5	9
12  6	10   6	10   2	6   2	6	10
3   7	11   7	11   3	7   3	7	11
4   8	12   8	12   4	8   4	8	12
after 8	after 12	after 4	after 8	afte	r 12



Some compilers can switch loop order (loop intercha In C the leftmost alternative will be the faster. Performance on three different systems. Full optimization on the compilers.

	System 1		System 2		System 3	
	$\mathbf{C}$	Fortran	$\mathbf{C}$	Fortran	$\mathbf{C}$	Fortran
By row	$0.12 \mathrm{~s}$	$0.093~{\rm s}$	$0.36 \ s$	$0.31 \mathrm{~s}$	$0.87~\mathrm{s}$	$2.9~\mathrm{s}$
By column	$1.32~{\rm s}$	$0.093~{\rm s}$	$1.08~{\rm s}$	$0.31 \mathrm{~s}$	$3.69~\mathrm{s}$	$0.68 \ s$

The first two Fortran compilers can switch loop order, the third cannot. Notice the difference between Fortran and C.

### Blocking and large strides

Sometimes loop interchange is of no use.

```
s = 0.0
do row = 1, n
    do col = 1, n
        s = s + A(row, col) * B(col, row)
    end do
end do
```

Blocking is good for data re-use, and when we have large strides.

Partition  ${\tt A}$  and  ${\tt B}$  in square sub-matrices each having the same order, the block size.

Treat pairs of blocks, one in A and one in B such that we can use the data which has been fetched to the L1 data cache. Looking at two blocks:



The block size must not be too large. Must be able to hold all the grey elements in A in cache (until they have been used).

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This code works even if n is not divisible by the block size).



n = 2000.

Note the speedups (4.5 and 7.2).

More on the BLAS (the Basic Linear Algebra Subprograms).

BLAS1: y := a\*x + y one would use daxpy

BLAS2: dgemv can compute y := a\*A\*x + b\*y

BLAS3: dgemm forms C := a\*A\*B + b\*C

daxpy:  $\mathcal{O}(n)$  data,  $\mathcal{O}(n)$  operations dgemv:  $\mathcal{O}(n^2)$  data,  $\mathcal{O}(n^2)$  operations dgemm:  $\mathcal{O}(n^2)$  data,  $\mathcal{O}(n^3)$  operations, data **re-use** 

Matrix multiplication: "row times column", slow. Blocking is necessary.



375 MHz machine, start two FMAs per clock cycle, top speed is 750 million FMAs per second.

LAPACK. Tuned libraries.

```
Indirect addressing, pointers
                                                               If-statements
Sparse matrices, PDE-meshes...
                                                               If-statements in a loop may stall the pipeline. Modern CPUs
Bad memory locality, poor cache performance.
                                                               and compilers are rather good at handling branches, so there
                                                                may not be a large delay.
  do k = 1, n
                                                                  Original version
                                                                                              Optimized version
    j = ix(k)
    y(j) = y(j) + a * x(j)
                                                                  do k = 1, n
                                                                                              take care of k = 1
  end do
                                                                    if (k == 1) then
                                                                                              do k = 2, n
                                                                      statements
                                                                                                statements for k = 2 to n
                                                                                              end do
                                                                    else
         system random ix ordered ix
                                         no ix
                                                                      statements
            1
                      39
                                  16
                                           9
                                                                    end if
            \mathbf{2}
                      56
                                 2.7
                                           2.4
                                                                  end do
                      83
            3
                                  14
                                           10
                                                                  if ( most probable ) then
                                                                  else if ( second most probable ) then
                                                                  else if ( third most probable ) then
                                                                    . . .
                                                               if (a(k) .and. b(k)) then, least likely first
                                                               if (a(k) .or. b(k)) then, most likely first
                           121
                                                                                           122
Inlining and overloading of operators
                                                                Alignment
Inlining: moving the body of a short procedure to the calling
routine. Here comes a slightly contrived example:
                                                                  integer*1 work(100001)
 module types
    type Point3D
                                                                  ! work(some_index) in a more general setting
      double precision :: x, y, z
                                                                  call do_work(work(2), 12500) ! pass address of work(2)
    end type Point3D
  end module types
                                                                  end
  function norm(point) result(res)
                                                                  subroutine do_work(work, n)
    use types
                                                                  integer
                                                                                     n
    type(Point3D)
                      :: point
                                                                  double precision work(n)
    double precision :: res
                                                                  work(1) = 123
    res = sqrt(point%x**2 + point%y**2 + point%z**2)
                                                                  . . .
  end
                                                               May produce "Bus error".
 program main
                                                                Alignment problems.
    ... code
  ! points is an array of type(Point3D)
                                                               It is usually required that double precision variables are stored
    do k = 1, MANY TIMES
                                                               at an address which is a multiple of eight bytes (multiple of four
      s = s + norm(points(k)) ! or something
                                                               bytes for a single precision variable).
                                  ! more realistic
    end do
    ... code
                                                               The slowdown caused by misalignment may easily be a factor
  end
                                                               of 10 or 100.
Changing norm(points(k)) in the main program to
sqrt(points(k)%x**2 + points(k)%y**2 + points(k)%z**2),
will give faster code.
Inlining, this way, by hand is error-prone, so a compiler can
usually do it for you. Some compilers are not doing a very good
job of it, though. It can make a difference if routines are stored
in different files.
                           123
                                                                                           124
```

Closing notes	Low level profiling
Two basic tuning principles:	valgrind and PAPI are two tools for counting cache misses.
• Improve the memory access pattern	http://valgrind.org/, man valgrind, and
– Locality of reference	/usr/share/doc/valgrind-3.1.1/html/index.html .
– Data re-use	From 22nd stanza in "Grímnismál" (poetic Edda). In old Ice-
Stride minimization, blocking, proper alignment and the avoidance of indirect addressing.	Valgrind heitir Valgrind den heter
• Use parallel capabilities of the CPU	er stendr velli á som varsnas på slätten,
– Avoid data dependencies	heilög fyr helgum dyrum; helig framför helig dörrgång; forn er sú grind, fornåldrig är grinden,
– Loop unrolling	en ∎at fáir vitu, och få veta,
<ul> <li>Inlining</li> <li>Elimination of if-statements</li> </ul>	nve non er i las lokin. nur non i las ar lyckt.
Choosing a good algorithm and a fast language, handling files	Valgrind is the lattice called.
in an efficient manner, getting to know ones compiler and using	in the plain that stands,
tuned libraries are other very important points.	holy before the holy gates: ancient is that lattice,
	but few only know
	The main gate of Valhall (Eng. Valhalla), hall of the heroes slain
	in battle.
	From the manual:
	"valgrind is a flexible program for debugging and profiling Linux executables. It consists of a core, which provides a synthetic
	CPU in software, and a series of "tools", each of which is a de- bugging or profiling tool."
	The memcheck tool performs a range of memory-checking func-
	tions, including detecting accesses to uninitialized memory, mis-
	use of allocated memory (double frees, access after free, etc.) and
125	detecting memory leaks.
We will use the cachegrind tool: cachegrind is a cache simulator. It can be used to annotate every	I refs: 46,146,658 Il misses: 756
line of your program with the number of instructions executed	L2i misses: 748
and cache misses incurred.	L2i miss rate: 0.00%
valgrindtool=toolname program args	$\mathbf{D}$ motor 21 072 427 (19 052 900 md+2 019 629 mm)
Call the following routine	D1 misses: 255,683 ( 130,426 rd+ 125,257 wr)
<pre>void sub0(double A[1000][1000], double *s)</pre>	L2d misses: 251,778 ( 126,525 rd+ 125,253 wr) D1 miss rate: 1.2% ( 0.7% + 4.1% )
{ int j, k, n = 1000;	L2d miss rate: 1.1% ( 0.7% + 4.1% )
*s = 0:	L2 refs: 256,439 ( 131,182 rd+ 125,257 wr)
5 – V)	L2 misses: 252,526 ( 127,273 rd+ 125,253 wr) L2 miss rate: 0.3% ( 0.1% + 4.1%)
for $(j = 0; j < n; j++)$ for $(k = 0; k < n; k++)$	valgrind produced the file cachegrind out 5796
*s += A[k][j];	(5796 is a pid). To see what source lines are responsible for the
}	cache misses we use cg_annotate -pid source-file. I have edited the listing and removed the columns dealing with the
Compile with -g:	instruction caches (the lines are too long otherwise).
I have edited the following printout:	% cg_annotate5796 sub.c
% valgrindtool=cachegrind a.out	br Dimr D2mr Dw Dimw D2mw
==5/96== Cachegrind, an I1/D1/L2 cache profiler. ==5796== Copyright (C) 2002-2005, and GNU GPL'd,	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
by Nicholas Nethercote et al.	3,002 0 0 1 0 for (j = ( 3,002,000 0 0 1.000 0 for (k = (
==5/96== For more details, rerun with: -v 9.990000e+08 6.938910e-01	7,000,000 129,326 125,698 1,000,000 0 $*s += A[k]$
	3 0 0 0 0 0 }
	Dr: data cache reads (1e. memory reads), D1mr: L1 data cache read misses D2mr: L2 cache data read misses Dw: D cache writes
	(ie. memory writes) Dlmw: L1 data cache write misses D2mw: L2 cache data write misses

To decrease the number of Dw:s we use a local summation variable (no aliasing) and optimze, -O3.

```
double local_s = 0;
for (j = 0; j < n; j++)
for (k = 0; k < n; k++)
local_s += A[k][j];
```

\*s = local\_s;

We can also interchange the loops. Here is the counts for the summation line:

Dr Dlmr D2mr 7,000,000 129,326 125,698 \*s += A[k][j]; previous 1,000,000 125,995 125,696 local\_s, -O3 1,000,000 125,000 125,000 above + loop interchange

Dw = D1mw = D2mw = 0.

valgrind cannot count TLB-misses, so switch to PAPI, which can.

PAPI = Performance Application Programming Interface

http://icl.cs.utk.edu/papi/index.html .

PAPI requires root privileges to install, so I have tested the code at PDC.

PAPI uses hardware performance registers, in the CPU, to count different kinds of events, such as L1 data cache misses and TLB-misses. Here is (a shortened example):

8	icc	main.c	sub.c
---	-----	--------	-------

% papiex -m -e	PAPI_L2_TCM -e PAPI_L1_TCM
-е	PAPI_TLB_DM/a.out
Processor:	Itanium 2
Clockrate:	900.000000
Real usecs:	52713
Real cycles:	47434686
Proc usecs:	52704
Proc cycles:	$474_{129}$ 33600

Note the drastic reduction of TLB-misses for the loop interchange. A local variable makes the code slightly faster. PAPI\_L1\_TCM: 814 PAPI\_L2\_TCM: 53345 PAPI\_TLB\_DM: 435949 Event descriptions: Event: PAPI\_L1\_TCM: L1 cache misses Event: PAPI\_L2\_TCM: L2 cache misses Event: PAPI\_TLB\_DM: Data TLB misses

The values change a bit between runs, but the order of magnitude stays the same. Here are a few tests. I call the function 50 times in a row. time in seconds.  $cycl = 10^9$  process cycles. L1, L2 and TLB in kilo-misses. local using a local summation variable.

	icc -00	icc -03	icc -03	icc -03	
			local	loop int	erc
time:	4.8	0.9	0.08	0.3	
cycl:	4.4	0.8	0.08	0.3	Giga
L1:	47	12	0.6	2.7	kilo
L2:	3883	3852	1697	3051	kilo
TLB:	24339	24559	22	23	kilo

time and cycl are almost the same, since the clockrate is 0.9 GHz. Note that the local summation variable, in column three, makes a dramatic difference. This is the case for loop inter change as well (column four) where we do not have a local summation variable (adding one gives essentially column three).

Here the same runs on a 3.3GHz, Intel Pentium 4 Model 3. We measure mega-misses (not kilo).

	icc -00	icc -03	icc -03	icc -03
			local	loop interc
time:	0.8	0.6	0.6	0.15
cycl:	2.8	2.0	2.1	0.5 Giga
L1:	50	48	49	41 Mega
L2:	2.8	3.2	3.3	2.7 Mega
TLB:	52	49	49	0.1 Mega
			130	

Here comes PAPI on the blocking example,  $s = s + \lambda(i, k) * B(k, j)$ , with ifort -03. n = 3000 and ten calls.

On the Itanium:

bs:	NO BL	16	32	64	
time:	2.6	1.3	1.1	1.9	
L1:	49	88	74	62	kilo
L2:	93792	22584	20491	21027	kilo
TLB:	91410	15365	9343	59165	kilo

On the Pentium with n = 5000 and ten calls:

NO BL	16	32	64	128	
10.2	3.4	2.5	2.2	3.1	
309	160	211	177	252	Mega
295	68	47	34	26	Mega
1066	102	64	103	262	Mega
	NO BL 10.2 309 295 1066	NO BL 16 10.2 3.4 309 160 295 68 1066 102	NO BL         16         32           10.2         3.4         2.5           309         160         211           295         68         47           1066         102         64	NO BL         16         32         64           10.2         3.4         2.5         2.2           309         160         211         177           295         68         47         34           1066         102         64         103	NO BL         16         32         64         128           10.2         3.4         2.5         2.2         3.1           309         160         211         177         252           295         68         47         34         26           1066         102         64         103         262

Note the drop in TLB-misses.